

Franco Santiago Caspe



📍 17 Rue Oscar et Jean Auriac, Bordeaux, France
☎ +34625744808
✉ francocaspe@gmail.com
🌐 <https://fcaspe.github.io>
📅 Date of birth: 8th July, 1993
🇨🇦🇮🇹 Nationality: Argentine and Italian

PROFILE

Master student in Computer Vision with a background on real time systems, deep learning, signal processing, heterogeneous computing and hardware engineering. I love music, travelling and meeting new people. I am looking forward to broadening my professional perspective with novel and impactful research.

EDUCATION

1 Sept 2019–Current

MSc in Image Processing and Computer Vision

Pazmany Peter Catholic University, Budapest, (Hungary)

Universidad Autónoma de Madrid, (Spain)

University of Bordeaux, (France)

- The two-year European Master in IPCV is conducted in three different universities, with the last semester being devoted to the realization of a thesis and a mandatory internship. This Master is strongly focused in machine learning and signal processing applied to image and video analysis/processing.

1 Mar 2012–20 Apr 2018

Electronic Engineer

Universidad Tecnológica Nacional, Bahía Blanca, (Argentina)

Average Marks: 94%

- **Ing. Isidoro Marín** Award received from the National Engineering Academy of Argentina. The Awards aim to publicly recognize those who have reached an outstanding level of scientific-technical training recognized by their University and the Academy.

EXPERIENCE

1 Dec 2019 - Current

Student Researcher on Quantized Neural Networks

Pazmany Peter Catholic University, Universidad Autónoma de Madrid, University of Bordeaux

- Analyzing quantization approaches in different convolutional and fully connected network architectures, targeting FPGAs for a highly parallelized operation. Studying knowledge transfer and training possibilities while evaluating the trade-off in accuracy, latency and power consumption the solutions present.

1 Sep 2018–1 Dec 2018

IAESTE Research Intern on Metamaterial Applications

Karunya Institute of Technology and Sciences, Coimbatore (India)

- Developed and simulated in HFSS a new cost-sensitive RF metamaterial unit cell, and then applied it on a low-profile 360-degree steerable micro-strip antenna design. Published paper with research team.

1 Nov 2017–1 Aug 2018

C++ Software Developer

Emtech S.A, Bahia Blanca (Argentina)

Working remotely for Hellastorm Inc. - Atlanta, USA.

- Designed a novelty HTTP parsing algorithm with pre-processing capabilities, for multi-core NIOS II operation. The algorithm is now being used for accelerating the application layer of a streaming server.
- Developed testing and validation utilities for a wide variety of FPGA modules.
- Created NVME bootstrap libraries and class interfaces for FPGA based Hosts, under Linux environment, needed to attach the drives to a HW-based host.

- 1 Dec 2015–1 Dec 2017 **Research and Development Intern**
Ministry of Defense of Argentina, Puerto Belgrano (Argentina)
- Developed software and firmware of a hard real time embedded system that operates as a gateway between a PC and the Warship's main computer.
 - Designed gateway's 4 and 6 layer PCB's. Designed VHDL to fit a new FPGA family and BGA footprint, as well as to feature multiple communication lanes.
- 1 Oct 2014–1 Apr 2016 **Teaching Auxiliary**
Universidad Tecnológica Nacional, Bahía Blanca (Argentina)
- Auxiliary in Algebra and Analytic Geometry, a first-year course in university.
- Provided valuable support to the students during their first year in University.

LANGUAGE SKILLS

- Spanish** Mother tongue.
- English** Level B2, Cambridge University First Certificate (July 2017).
Currently I am a student in an English taught MSc programme.
- Italian** Level B2, CILS International Certificate.

PEER-REVIEWED PUBLISHED ARTICLES

- October 2019 **Metasurface based pattern reconfigurable antenna for 2.45 GHz ISM band applications**
International Journal of RF and microwave computer-aided engineering.
<https://doi.org/10.1002/mmce.22007>
- October 2017 **Gateway for data transferring between real time and deferred time domains**
Published in Spanish. Proceedings of "VIII Congreso de Microelectrónica Aplicada".
- August 2017 **A real time F0 estimator based on the YIN algorithm**
Published in Spanish. Proceedings of CASE 2017. ISBN: 978-987-46297-3-9.
- August 2016 **A real-time network interface test bench**
Published in Spanish. Proceedings of CASE 2016. ISBN: 978-987-45523-8-9.
Outstanding work mention.

PERSONAL PROJECTS

- August 2020 **dx7pytorch**
Musical instrument dataset synthesized on-the-fly.
<https://github.com/fcaspe/dx7pytorch>
- April 2020 **Melopak**
A tool for generating musical instrument datasets over MIDI.
<https://github.com/fcaspe/melopak>
- January 2019 – August 2019 **bFreeOrgan2**
Drawbar organ synthesizer, for Linux and Cortex M4 microcontroller.
<https://github.com/fcaspe/bfreeOrgan2>
- March 2017 - August 2017 **Intromision: An Album by Lo Barato Sale Caro**
This is the first EP of my music band. Link to the Album:
<https://lobaratosalecaro.bandcamp.com/releases>